Inventor: Gang ZHANG et al. Title: ANALOG INTEGRATED CIRCUIT LAYOUT DESIGN Replacement Sheet 1 of 6 Start Fig 1 Input Circuit topology, performance specs. and tolerances Input circuit constraints on relative Utilize relationship(s) defined in Utilize relationship(s) defined in placement of circuit step 12 for parasitic effects step 12 for device parameter devices with respect variations to determine for the variations to determine for the to each other change in each parasitic effect a change in each device parameter a corresponding change in at least corresponding change in at least one performance specification. one performance specification. Define initial layout of devices including initial device sizes and routing of Determine change in at interconnecting least one parasitic effect 24 conductors due to rerouting of the Determine a change in at one conductor 10 least one device parameter of each Determine device resized circuit device. parameter variations, parasitic electrical Reroute at least one effect variations and 22 conductor to the performance repositioned circuit variations. device 12 Resize each chosen circuit device 30 Define relationships between Reposition each performance variations, device chosen circuit parameter variations and device. between performance variations and parasitic effect 28 variations. Choose at least Choose at least one circuit one circuit device. device. Reposition Resize 14 Are circuit performances Resize or within predetermined reposition one tolerances of or more circuit performance devices? specifications? Ye s Stop

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